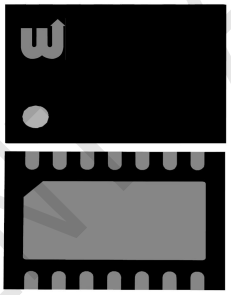
WSTD5070AN-L

Smart High-Side Power Switch Dual Channel，70mΩ，DFN9×6-14L ，*AEC-Q100 qualified*

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 24 V and 48 V trucks + trailer and transportation systems

Package	DFN9×6-14L
Marking	WSTD5070AN-L



AEC Qualified

RoHS

ISO 26262 ready

Halogen-free

Features

- PRO-SIL™ ISO 26262-ready for supporting the integrator in evaluation of hardware element according to ISO 26262:2018 Clause 8-13
- Dual channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Optimized electromagnetic compatibility
- Very low electromagnetic susceptibility
- User adjustable current limitation

Diagnostic Functions

- Off-state open load detection
- OUT short to VS detection
- Overload and short to ground latch-off
- Thermal shutdown latch-off

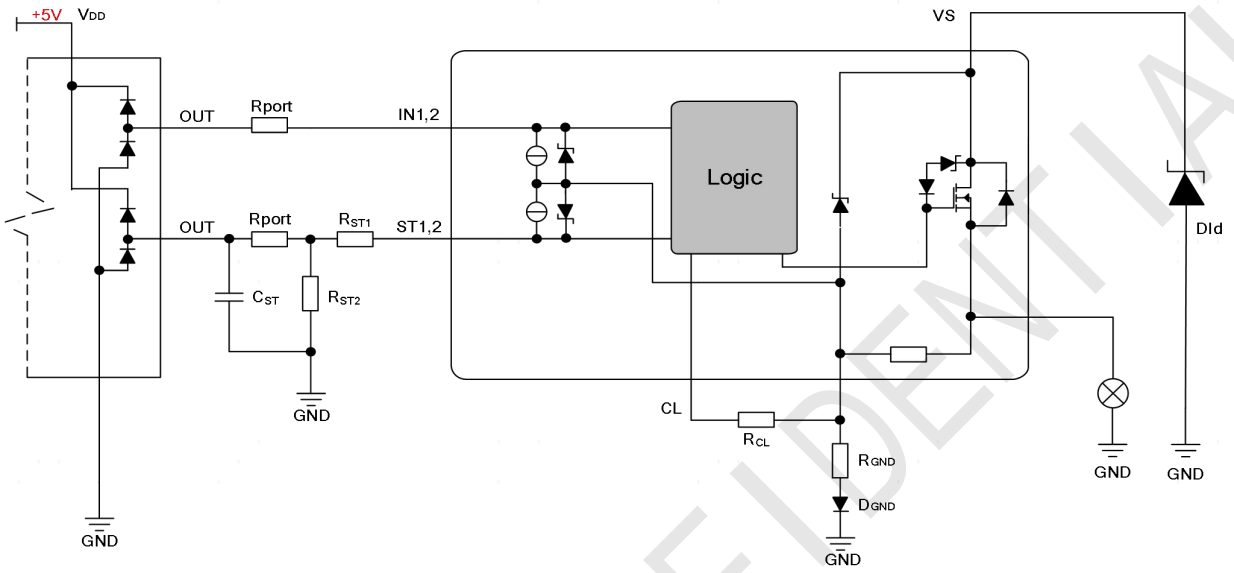
Protection Functions

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of VS
- Thermal shutdown
- Electrostatic discharge protection

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage(T_j≥25 °C)	V_S	70V
Operating voltage range	V_{NOM}	5-58V
On-state resistance (per channel，T_j = 25℃)	R_{ON}	70mΩ
Nominal load current (one channel active，T_j = 25℃)	$I_{L(NOM)1}$	4A
Nominal load current (All channels active，T_j = 25℃)	$I_{L(NOM)2}$	3A
Current limitation	I_{LIMH}	Adjustable
Supply current in sleep	I_{SLEEP}	5uA

Typical Application Circuit



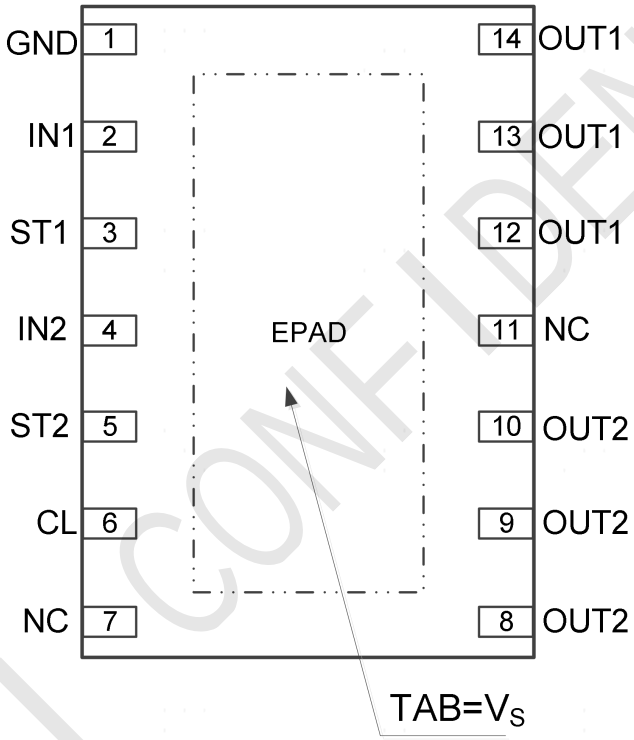
Note1：For D_{GND}, the diode with lower V_F is advisable.

Ordering Information

Package	Top Mark	Part No.
DFN9×6-14L, Pb-free	WSTD5070ANL XXYMXX	WSTD5070AN-L

Pin Configuration

Top view



Pin Description

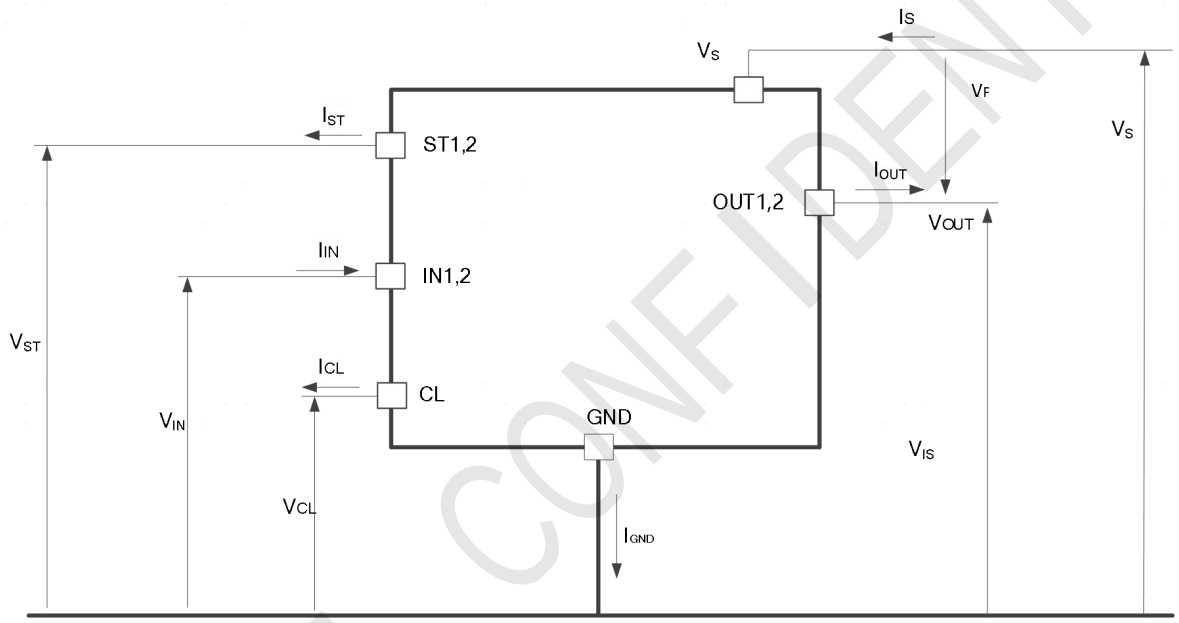
Pin Name	Pin NO.	Pin Description
GND	1	Ground connection. Must be reverse battery protected by an external diode / resistor network.
IN1/2	2/4	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
ST1/2	3/5	Diagnostic feedback of channel.
CL	6	Adjustable current limit, floating if external current limit is not need.
NC	7/11	Not Connected
OUT2	8/9/10	Power outputs.
OUT1	12/13/14	
VS	EPAD	Battery connection.

Table 1. Suggested connections for unused and not connected pins

Connection / pin	OUT1,2	IN1,2
Floating	X(1)	X
To ground	Not allowed	Through 15K resistor

Note2：X do not care.

Current and Voltage Conventions



Note3: $V_F = V_{OUT} - V_S$ during reverse battery condition.

Absolute Maximum Ratings (Note4)

Symbol	Parameter	Value	Unit
V_s	Transient supply voltage	65	V
$-V_s$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	50	mA
I_{OUT}	OUT1,2 DC output current	Internally limited	A
V_{IN}, V_{CL}	IN1,2, CL DC input voltage	-0.3 to 6.0	V
T_j	Junction operating temperature	-40 to 150	℃
T_{stg}	Storage temperature	-55 to 150	

Note4：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Thermal Resistance (Note5)

Symbol	Parameter	Value	Unit
T_{JC}	Thermal Resistance Junction-to-Case	1.3	℃/W
T_{JA}	Junction-to-Ambient Thermal Resistance	25	℃/W

Note5：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

ESD Susceptibility (Note6)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}$ 3)	ESD Susceptibility all Pins (HBM)	±2	kV
$V_{ESD(HBM)\_OUT}$	ESD Susceptibility OUT vs GND and V_S connected (HBM)	±4	kV
$V_{ESD(CDM)}$ 4)	ESD Susceptibility all Pins (CDM)	±500	V
$V_{ESD(CDM)\_CRN}$	ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	±750	V

Note6：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.

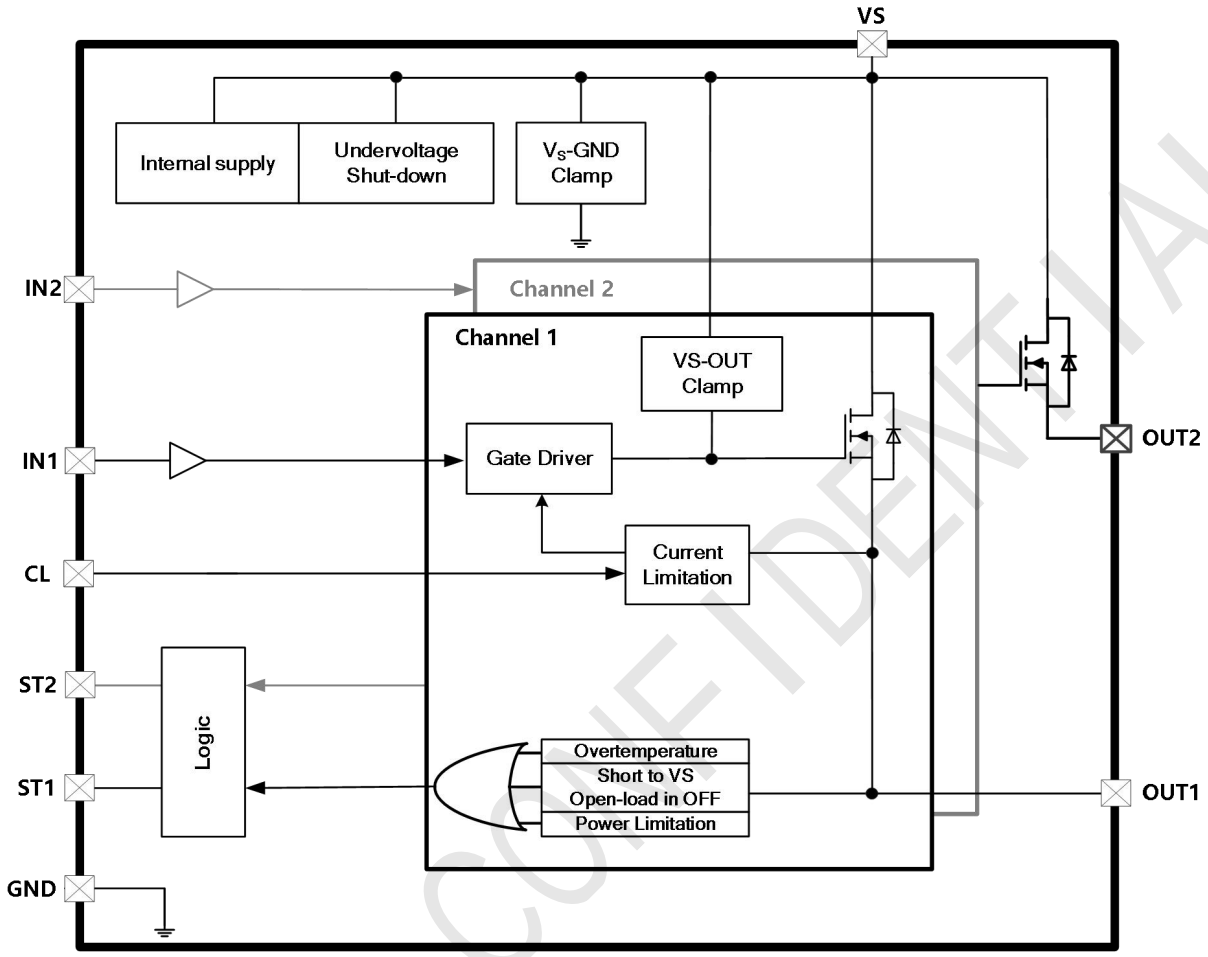
4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

EAS Susceptibility (Note7)

Symbol	Parameter	Values			Unit	Note or Test Conditon
		Min.	Typ.	Max.		
E_{AS}	Maximum Energy Dissipation Single Pulse (one channel)			90	mJ	I_{OUT} = 4A $T_{J(0)}$ = 150 °C V_S = 48V

Note7：Not subject to production test - specified by design.

Functional Block



Electrical Characteristics (Note8) , 5V < V_S < 58 V; -40°C < Tj < 150°C, unless otherwise specified

Power section

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Nominal operating voltage	V_{NOM}		5	48	58	V
Under voltage shutdown	V_{USD}			3.5	4.5	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	I_{OUT}=2A, T_j = 25℃		70		mΩ
		I_{OUT}=2A,T_j =150℃			140	
		I_{OUT}=2A,V_S =5V, T_j = 25℃			110	
Nominal load current (One Channel Active)	$I_{L(NOM)1}$	T_A=25℃		4		A
Nominal load current at T_A=85℃ (One Channel Active)	$I_{L(NOM)1\_85}$	T_A=85℃, T_j < 150℃		3		A
Nominal load current (All Channels Active)	$I_{L(NOM)2}$	T_A=25℃		3		A
Nominal load current at T_A=85℃ (All Channels Active)	$I_{L(NOM)2\_85}$	T_A=85℃, T_j < 150℃		2		A
Inverse Current Capability	$I_{L(INV)}$	V_S<V_{OUT}, V_{IN}=5V, T_A=25℃		4		A
V_S clamp voltage	V_{CLAMP}	I_S=20 mA	70	75		V
Supply current in sleep	I_{SLEEP}	V_S=48V, V_{IN}=V_{OUT}=0V, T_j =25℃		5.0	10	μA
		V_S =48V, V_{IN}=V_{OUT} =0V, T_j= 125℃			25	μA
Control stage current consumption in ON state	$I_{GND(ON)}$	V_S=48V,$V_{IN1,2}$=5V		8.0	16	mA
Off-state output current	$I_{L(off)}$	V_{IN} =V_{OUT}=0V, V_S=60V, T_j =25℃		5	10	μA
		V_{IN} =V_{OUT}=0V, V_S=60V, T_j =125℃			20	μA
OUT - V_S diode voltage	V_F	I_{OUT} =-2A, T_j =150℃			0.9	V

Switching

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at T_j = 25℃	$T_{d\ (on)}$	V_S=48V,R_L=24Ω		10	40	us
Turn-off delay time at T_j = 25℃	$T_{d\ (off)}$			25	80	us
Turn-on voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{on}$	V_S=48V,R_L=24Ω	0.5	1.2	2.5	V/us
Turn-off voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{off}$		0.5	1.5	3.0	
Differential pulse skew(t_{PHL} - t_{PLH})	t_{SKEW}	V_S=48V,R_L=24Ω	-50		50	us

Logic input (IN1,2)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_{LOW}				0.9	V
Low level logic input current	I_{LOW}	V_{LOW}=0.9V	2	11	35	uA
Logic input high level voltage	V_{HIGH}		2.1		6.0	V

High level logic input current	I_{HIGH}	V_{HIGH}=2.0V	1	10	32	uA
Logic input hysteresis voltage	$V_{(hyst)}$			0.2		V
ST low voltage	V_{ST}	I_{ST} = +1.6 mA			0.6	V
ST high voltage	V_H	I_{ST} = +1.6 mA			6.0	V

Protections

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CL-pin voltage V_{CL} (in ON- state)	V_{CL}	V_S=48V, V_{IN}=5V	0.57	0.6	0.63	V
Allowed I_{CL} range for adjusting current limit threshold	$I_{CL-range}$	V_S=48V,V_{IN}=5V	5		150	uA
CL short to device ground current	$I_{CL-short}$	V_S=48V,V_{IN}=5V	-50%	360	+50%	uA
DC short circuit current	I_{LIMH}	5V < V_S< 36V	5	7.5	10	A
		V_S=48V,V_{IN}=5V，R_{CL}=8.2K	-20%	4.8	+20%	
		V_S=48V,V_{IN}=5V，R_{CL}=12K	-20%	3.6	+20%	
		V_S=48V,V_{IN}=5V，R_{CL}=24.9K	-20%	2.4	+20%	
		V_S=48V,V_{IN}=5V，R_{CL}=120K	-20%	1.4	+20%	
Shutdown temperature	T_{TSD}		150	175	200	℃
Thermal hysteresis	T_{HYST}			20		℃
Current limit reset temperature	T_R			135		℃
Dynamic temperature	ΔT_{J_SD}	T_j = -40℃		60		℃
Turn-off output voltage clamp	V_{DEMAG}	I_{OUT}=1A, L= 3mH, T_j =-40℃ to 150℃	V_S-68	V_S-73		V

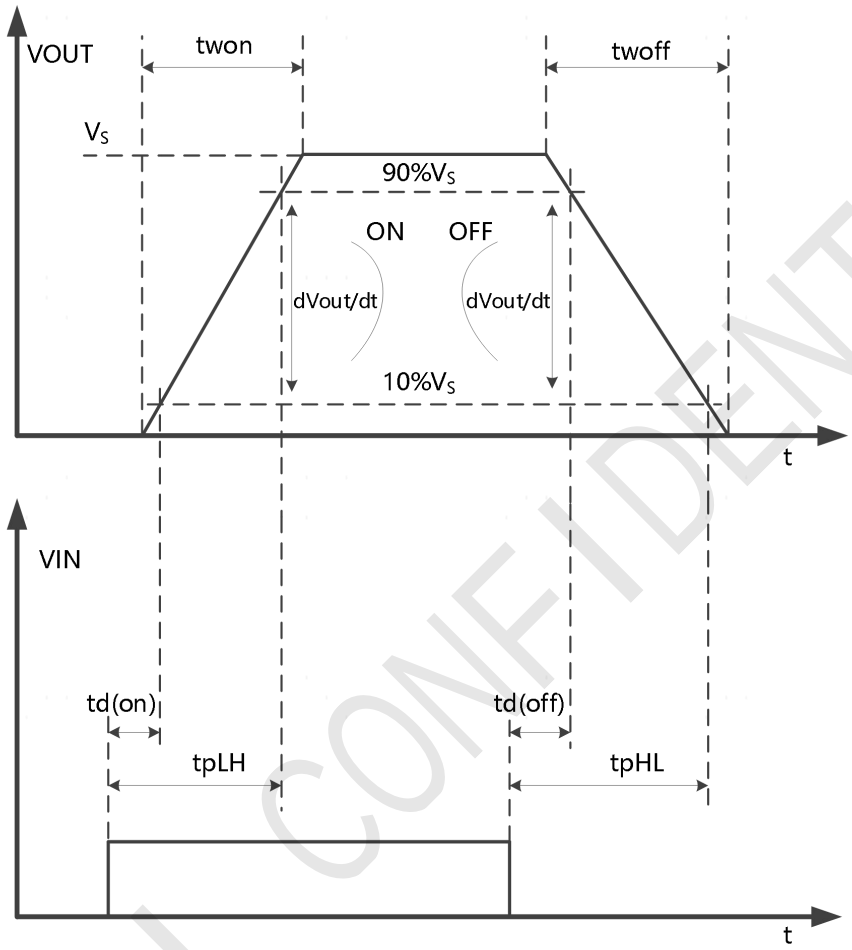
OFF-state diagnostic

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF-state open load voltage detection threshold	V_{OL}	V_{IN}=0V	2	3.5	5	V
OFF-state output sink current	$I_{L(off2)}$	V_S=48V,V_{IN} = 0V, V_{OUT}=V_{OL}, T_j = -40℃ to 150℃		-30		uA
OFF-state diagnostic delay time from falling edge of IN	t_{DSTKON}	V_{IN1}= 5V to 0V, V_{OUT1} =5V	150	400	800	us

Note8: Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

Switching Status and Timing Relationship

Switching time and pulse skew



T_{DSTKON}

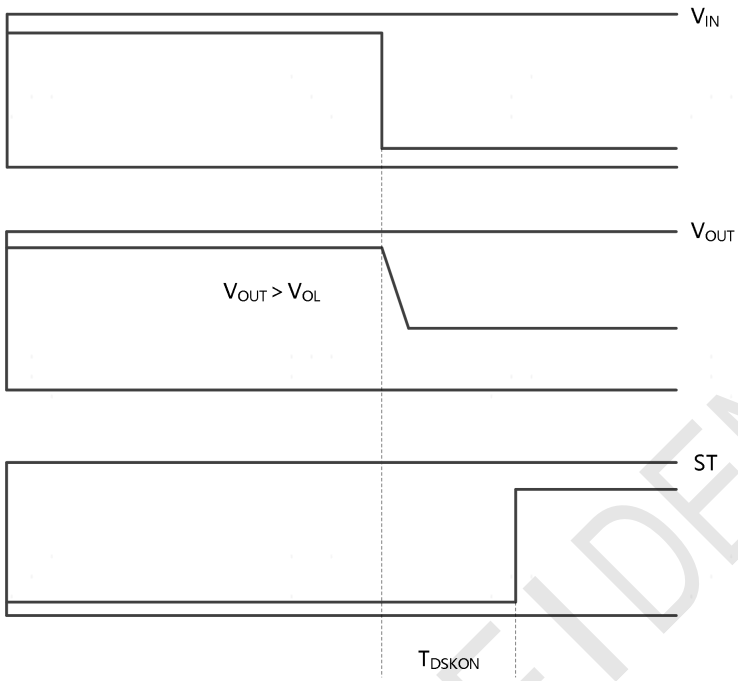
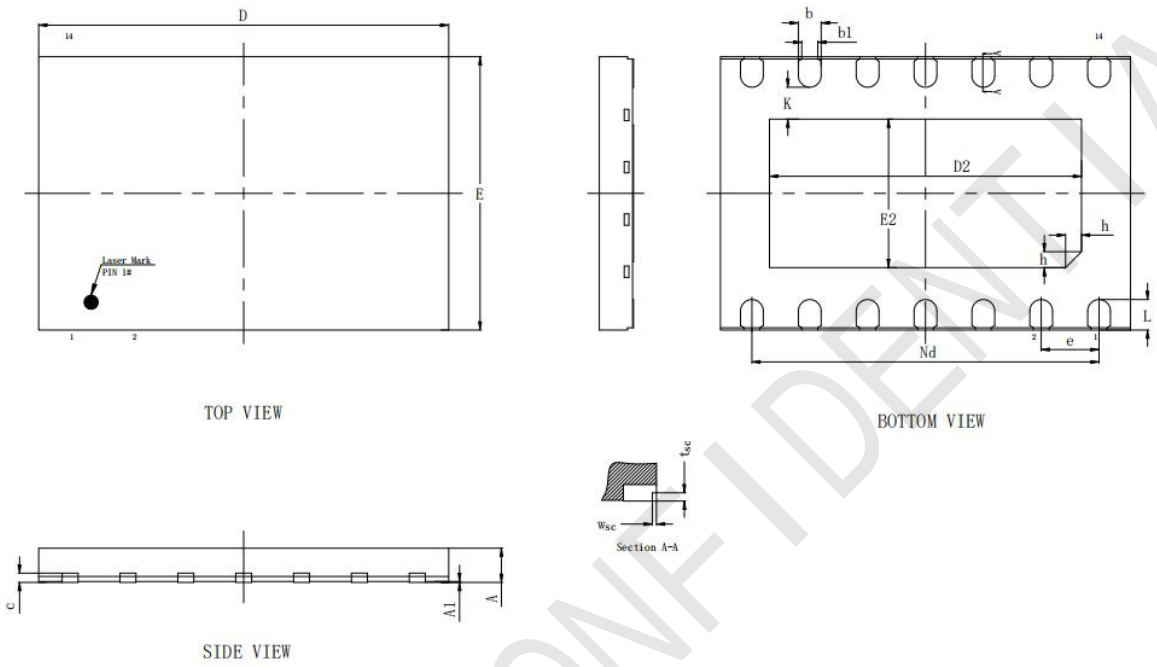


Table 2. Truth table

Conditions	IN_X	OUT_X	ST_X
Normal	L	L	L
	H	H	L
Over Temperature	H	L	H
Open-Load	L	H	H

Package Outline

DFN9×6-14L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.45	0.50	0.55
b1		0.35REF	
c		0.203REF	
D	8.90	9.00	9.10
D2	6.75	6.85	6.95
e		1.27BSC	
Nd		7.62BSC	
E	5.90	6.00	6.10
E2	3.16	3.26	3.36
L	0.62	0.67	0.72
h	0.30	0.35	0.40
K		0.70REF	
W_{SC}	0.01	-	0.09
t_{SC}	0.08	-	0.18

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