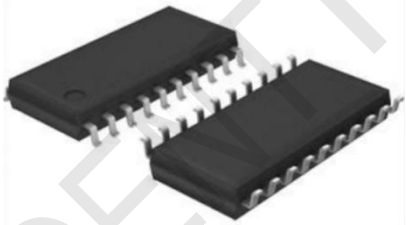
WSTQ724G

Smart High-Side Power Switch Quad Channel，80mΩ， *AEC-Q100 qualified*

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 12 V and 24 V trucks + trailer and transportation systems

Package	SOP-20L
Marking	WSTQ724G



AEC Qualified

RoHS

ISO 26262 ready

Halogen-free

Basic Features

- Quad channel device
- Very low stand-by current
- 3V and 5 V compatible logic inputs
- Optimized electromagnetic compatibility
- Very low electromagnetic susceptibility

Diagnostic Functions

- Open load detection in OFF-state
- Output short to Vbb detection
- Feedback of thermal shutdown in ON-state

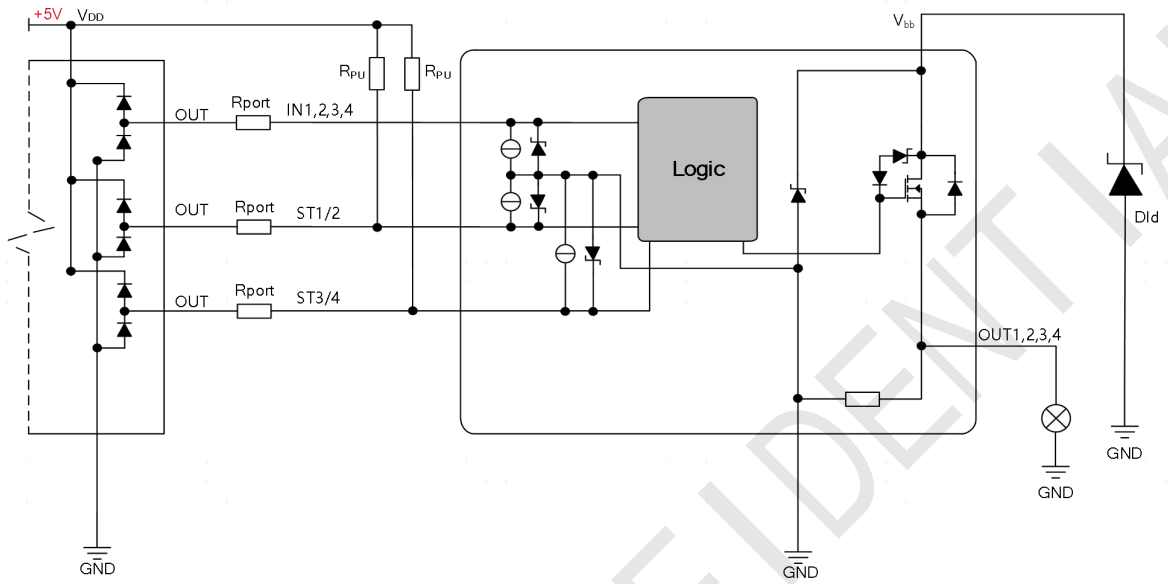
Protection Functions

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of Vbb
- Thermal shutdown
- Electrostatic discharge protection

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage	V_{bb}	58V
Operating voltage range	V_{NOM}	5-40V
On-state resistance (per channel)	R_{ON}	80mΩ
Nominal load current (one channel active)(T_A=25°C)	$I_{L(NOM)1}$	3A
Nominal load current (All channels active)(T_A=25°C)	$I_{L(NOM)2}$	8A
Current limitation(per channel)	I_{LIMH}	12A
Supply current in sleep	I_{SLEEP}	3uA

Typical Application Circuit

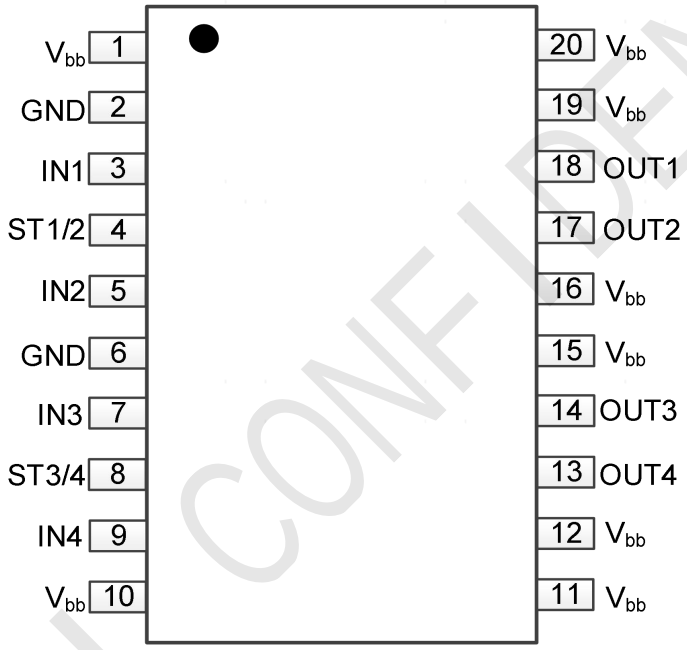


Ordering Information

Package	Top Mark	Part No.
SOP-20L, Pb-free	WSTQ724G XXYMXX	WSTQ724G

Pin Configuration

Top view



Pin Description

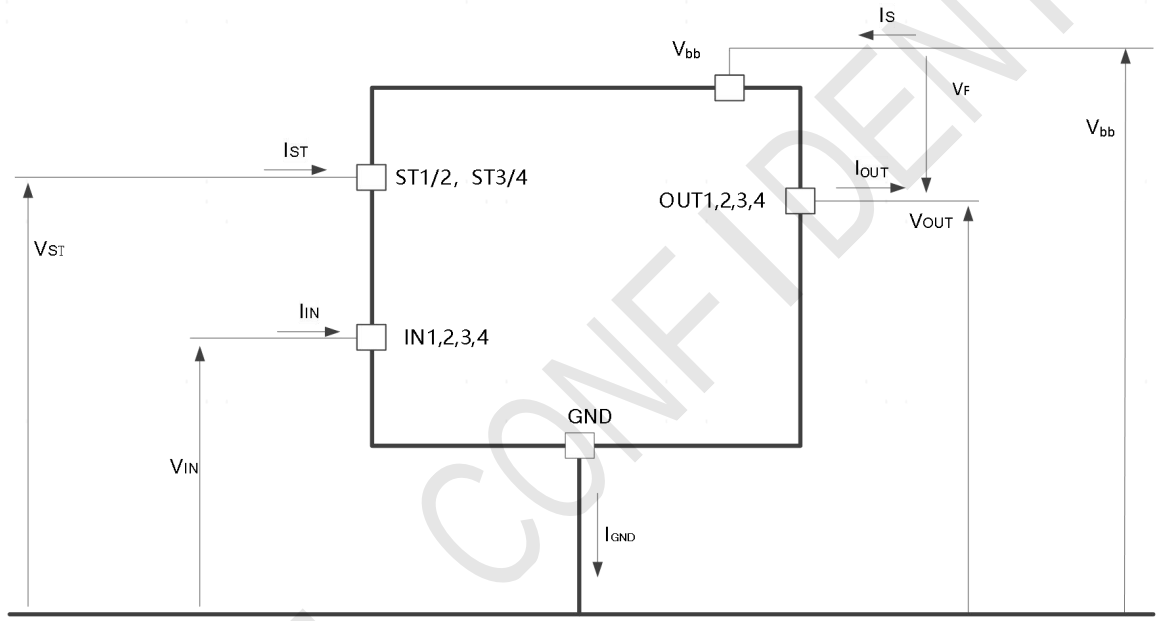
Pin Name	Pin NO.	Pin Description
V_{bb}	1/10/11/12/15/16/19/20	Battery connection.
GND	2/6	Ground connection.
IN/1/2/3/4	3/5/7/9	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
ST1/2	4	Diagnostic feedback of of channel 1,2
ST3/4	8	Diagnostic feedback of of channel 3,4
OUT1/2/3/4	13/14/17/18	Power outputs.

Table 1. Suggested connections for unused and not connected pins

Connection / pin	OUTPUT	INPUT
Floating	X(1)	X
To ground	Not allowed	Through 15K resistor

Note1：X do not care.

Current and Voltage Conventions



Note2: $V_F = V_{OUT} - V_{bb}$ during reverse battery condition.

Absolute Maximum Ratings (Note3)

Symbol	Parameter	Value	Unit
V_{bb}	Transien supply voltage	58	V
$-V_{bb}$	Reverse DC supply voltage	-35	V
V_{bb}	Supply voltage for full short circuit protection ($T_{j,start}$=-40℃-150°C)	36	V
I_{OUT}	OUT1,2,3,4 DC output current	Internally limited	A
V_{IN}	IN1,2,3,4, DC input voltage	-9 to 6.0	V
$V_{ST1/2}$，$V_{ST3/4}$	ST1/2，ST3/4，DC input voltage	-9 to 6.0	V
T_j	Junction operating temperature	-40 to 150	℃
T_{stg}	Storage temperature	-55 to 150	

Note3：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Thermal Resistance (Note4)

Symbol	Parameter	Value	Unit
T_{JC}	Thermal Resistance Junction-to-Case	1.3	℃/W
T_{JA}	Junction-to-Ambient Thermal Resistance	35	℃/W

Note4：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

ESD Susceptibility (Note5)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}$ 3)	ESD Susceptibility all Pins (HBM)	±2	kV
$V_{ESD(HBM)\_OUT}$	ESD Susceptibility OUT vs GND and V_{bb} connected (HBM)	±4	kV
$V_{ESD(CDM)}$ 4)	ESD Susceptibility all Pins (CDM)	±500	V
$V_{ESD(CDM)\_CRN}$	ESD Susceptibility Corner Pins (CDM) (pins 1, 10,11, 20)	±750	V

Note5：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.

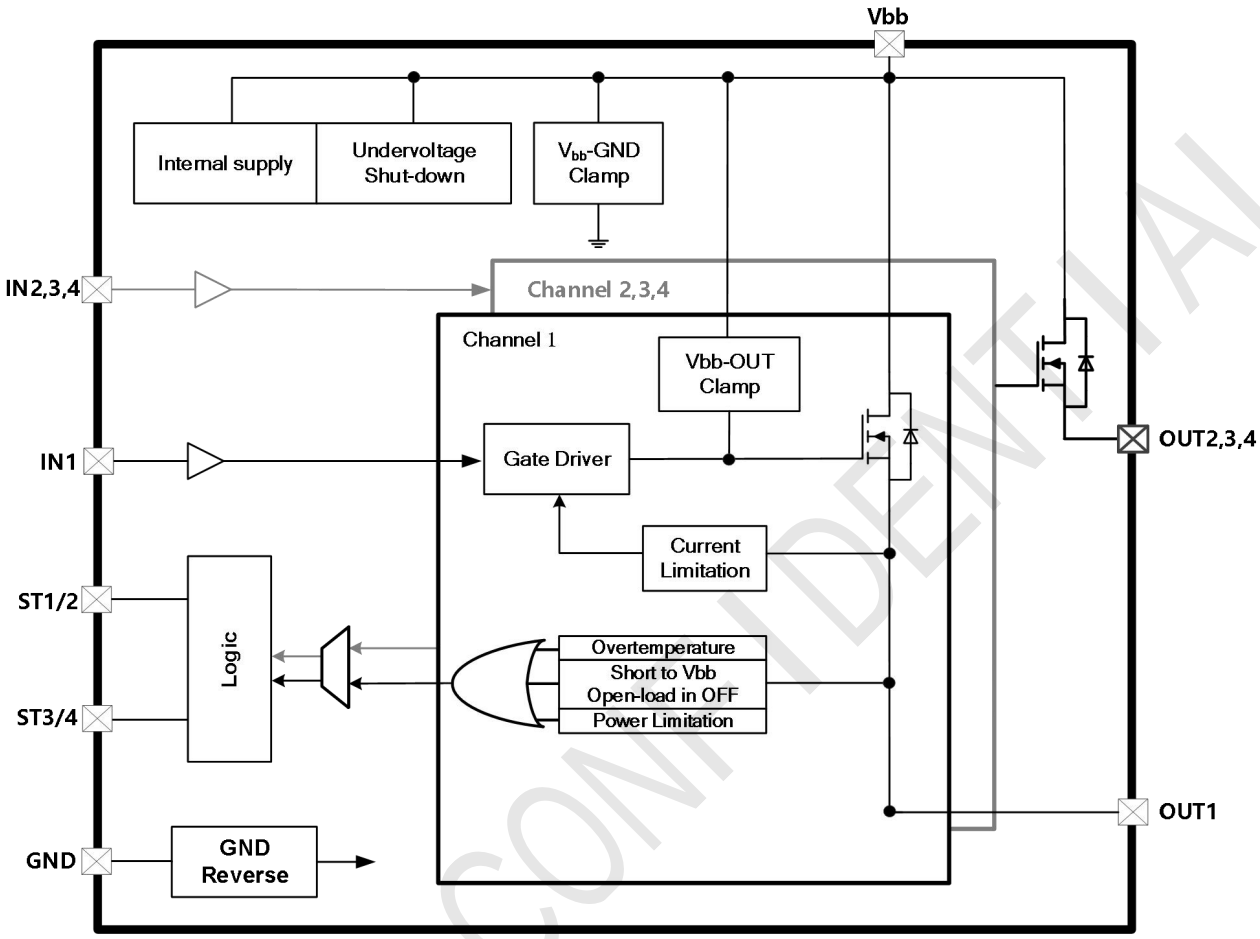
4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

EAS Susceptibility (Note6)

Symbol	Parameter	Values			Unit	Note or Test Conditon
		Min.	Typ.	Max.		
E_{AS}	Maximum Energy Dissipation Single Pulse (one channel)			120	mJ	I_{OUT} = 5A $T_{J(0)}$ = 150 °C V_S = 28 V

Note6:：Not subject to production test - specified by design.

Functional Block



Electrical Characteristics (Note7) , 5V<Vbb < 40 V; -40°C < Tj < 150°C, unless otherwise specified

Power section

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Nominal operating voltage	V_{NOM}		5	24	40	V
Under voltage shutdown	V_{USD}			3.5	5.0	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	I_{OUT}=1A, T_j = 25℃		80		mΩ
		I_{OUT}=1A,T_j =150℃			160	
		I_{OUT}=1A,V_{bb} =4.5V, T_j = 25℃			120	
Nominal load current (One Channel Active)	$I_{L(NOM)1}$	T_A=25℃		3		A
Nominal load current at T_A=85℃ (One Channel Active)	$I_{L(NOM)1\_85}$	T_A=85℃, T_j < 150℃		2		A
Nominal load current (All Channels Active)	$I_{L(NOM)2}$	T_A=25℃		8		A
Nominal load current at T_A=85℃ (All Channels Active)	$I_{L(NOM)2\_85}$	T_A=85℃, T_j < 150℃		6		A
Inverse Current Capability	$I_{L(INV)}$	V_{bb} <V_{OUT}, V_{IN}=5V, T_A=25℃		3		A
V_{bb} clamp voltage	V_{CLAMP}	I_S=20 mA	58	64	71	V
Supply current in sleep	I_{SLEEP}	V_{bb} =36V, V_{IN}=V_{OUT}=0V, T_j =25℃		3.0	6.0	μA
		V_{bb} =36V, V_{IN}=V_{OUT}=0V, T_j= 125℃			20	μA
Sleepy mode blanking time	t_{D_SLEEP}	V_{bb} =36V, V_{OUT}=0V V_{IN}=5V to 0V	150	400	800	us
Control stage current consumption in ON state	$I_{GND(ON)}$	V_{bb} =36V, V_{INx}=5V, one channel ON		3.0	6.0	mA
		V_{bb} =36V, $V_{IN1,2,3,4}$=5V, all channels ON		8.0	16	mA
Off-state output current	$I_{L(off)}$	V_{IN} =V_{OUT}=0V, V_{bb} =36V, T_j =25℃	0	0.1	3	μA
		V_{IN} =V_{OUT}=0V, V_{bb} =36V, T_j =125℃	0		6	μA
Output - V_{bb} diode voltage	V_F	I_{OUT} =-2A, T_j =150℃			0.9	V

Switching

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at T_j = 25℃	$T_{d\ (on)}$	V_{bb}=28V,R_L=28Ω		10	30	us
Turn-off delay time at T_j = 25℃	$T_{d\ (off)}$			25	70	us
Turn-on voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{on}$	V_{bb}=28V,,R_L=28Ω	1.0	2.0	4.0	V/us
Turn-off voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{off}$		1.0	2.5	5.0	
Differential pulse skew(t_{PHL} - t_{PLH})	t_{SKEW}	V_{bb}=28V,R_L=28Ω	-50		50	us

Logic input (IN1,2,3,4，ST1/2，ST3/4)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_{LOW}				0.9	V
Low level logic input current	I_{LOW}	V_{LOW}=0.9V	2	11	35	uA
Logic input high level voltage	V_{HIGH}		2.1		6.0	V
High level logic input current	I_{HIGH}	V_{HIGH}=2.0V	1	10	32	uA
Logic input hysteresis voltage	$V_{(hyst)}$			0.2		V
ST low voltage	V_{ST}	I_{ST} = +1.6 mA			0.6	V
ST high voltage	V_H	I_{ST} = +1.6 mA			6.0	V

Protections

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DC short circuit current	I_{LIMH}	5V < V_{bb}< 36V ,V_{DS}=6V	8	12	18	A
		V_{DS}=32V		8		
Short circuit current during thermal cycling	I_{LIML}	V_{bb}=24V, T_R<T_j<T_{TSD}.		4		
Shutdown temperature	T_{TSD}		150	175	200	℃
Thermal hysteresis	T_{HYST}			20		℃
Current limit reset temperature	T_R			135		℃
Dynamic temperature	ΔT_{J_SD}	T_j = -40℃		60		℃
Turn-off output voltage clamp	V_{DEMAG}	I_{OUT}=2A, L= 3mH, T_j =-40℃ to 150℃	V_{bb}-58	V_{bb}-64	V_{bb}-71	V

OFF-state diagnostic

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF-state open load voltage detection threshold	V_{OL}	V_{INx}=0V	2	3	4	V
OFF-state output sink current	$I_{L(off2)}$	V_{INx} = 0V, V_{OUT}=4V,T_j = -40℃ to 150℃		-15		uA
OFF-state diagnostic delay time from falling edge of IN	t_{DSTKON}	V_{INx} = 5V to 0V, V_{OUT} =4V	150	400	800	us

Note7: Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

Switching Status and Timing Relationship

Switching time and pulse skew

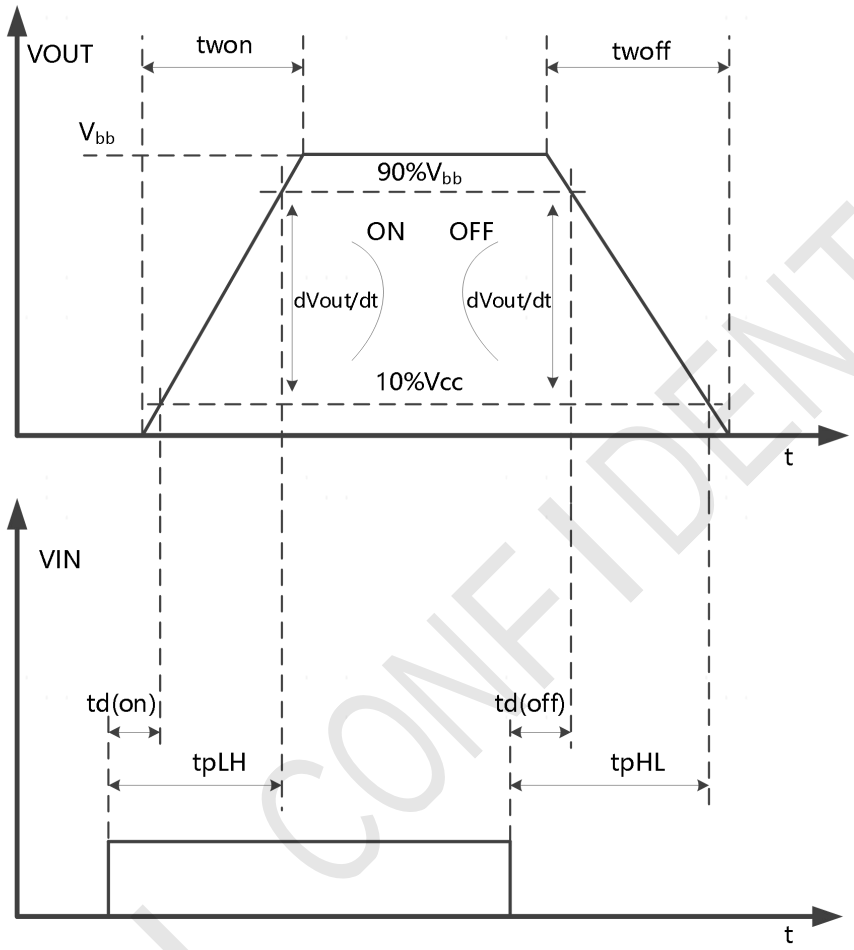
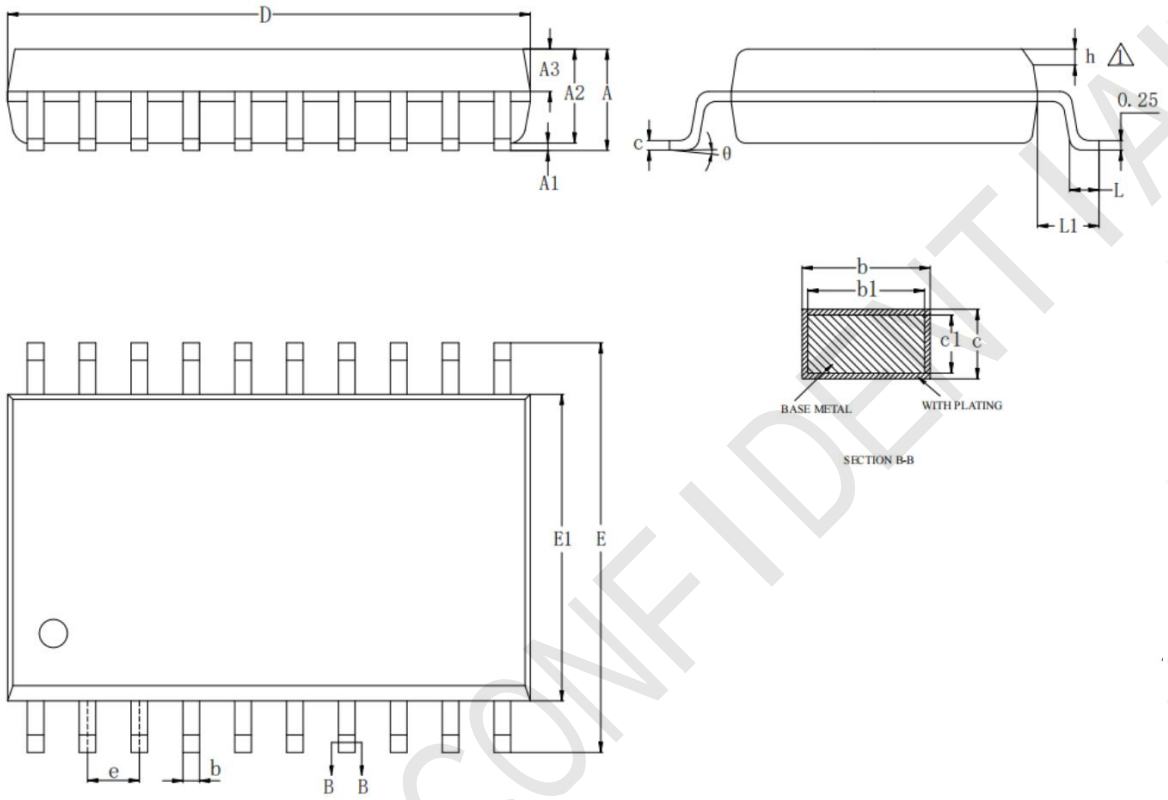


Table 2. Truth table

Conditions	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	ST1/2	ST3/4
Normal	L	L	L	L	L	L	L	L	H	H
	H	L	L	L	H	L	L	L	H	H
	.....									
	H	H	H	H	H	H	H	H	H	H
Over Temperature	H	X	X	X	L	X	X	X	L	H
	X	H	X	X	X	L	X	X	L	H
	X	X	H	X	X	X	L	X	H	L
	X	X	X	H	X	X	X	L	H	L
Open-Load	L	X	X	X	H	X	X	X	L	H
	X	L	X	X	X	H	X	X	L	H
	X	X	L	X	X	X	H	X	H	L
	X	X	X	L	X	X	X	H	H	L

Package Outline

SOP-20L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	—	1.00
L1	1.40REF		
θ	0	—	8°
h	0.50REF		

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